

### Product Description

The Nxbeam NPA2002-DE is a Ka-band high power amplifier MMIC fabricated in 0.2um GaN HEMT on SiC. The MMIC operates from 27 to 30 GHz and provides an average of 34 W saturated output power, 31% PAE, and 25 dB of linear gain. The NPA2002-DE comes in die form with RF input and output matched to 50  $\Omega$  with DC blocking capacitors for easy system integration. The HEMT devices are fully passivated for reliable operation.



### Key Features

- Frequency: 27 – 30 GHz
- Linear Gain (Ave.): 25 dB
- Psat (Ave.): 34 W
- PAE (Ave.): 31%
- Chip Dimensions: 4.975 x 3.975 x 0.1 mm

### Applications

- Ka-band Satellite Communications
- 5G Infrastructure
- Point-to-Point/Multipoint Digital Radios

### Electrical Specifications

Test Condition:  $V_d = 24$  V,  $I_{dq} = 2.0$  A, CW Performance in Fixture, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		27		30	GHz
Gain (Small Signal)	27 GHz		25.5		dB
	28 GHz		25.2		
	29 GHz		24.9		
	30 GHz		25.2		
Output Power (at Psat, Pin=26 dBm)	27 GHz		46.0		dBm
	28 GHz		45.4		
	29 GHz		44.9		
	30 GHz		45.0		
PAE (at Psat, Pin=26 dBm)	27 GHz		33.1		%
	28 GHz		30.8		
	29 GHz		28.6		
	30 GHz		29.6		
Power Gain (at Psat, Pin=26 dBm)	27 GHz		20.7		dB
	28 GHz		20.5		
	29 GHz		19.6		
	30 GHz		20.1		
Input Return Loss	27 GHz		15		dB
	28 GHz		12		
	29 GHz		20		
	30 GHz		18		
Output Return Loss	27 GHz		13		dB
	28 GHz		17		
	29 GHz		15		
	30 GHz		14		

### Maximum Quiescent Bias

Parameter	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)	28	V
Drain Current (Id1)	264	mA
Drain Current (Id2)	640	mA
Drain Current (Id3)	2112	mA

Maximum quiescent bias represents the operational bias used during reliability life testing. Biasing the part at or below this bias ensures reliability will be bound by the published reliability results.

### Absolute Maximum Ratings (Temp. = 25°C)

Parameter	Min	Max	Unit
Drain Voltage (Vd1, Vd2, Vd3)		28	V
Drain Current (Id1)		660	mA
Drain Current (Id2)		1600	mA
Drain Current (Id3)		5250	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V

Absolute maximum ratings represent the maximum current under power saturation conditions.

### Recommended Quiescent Operating Condition

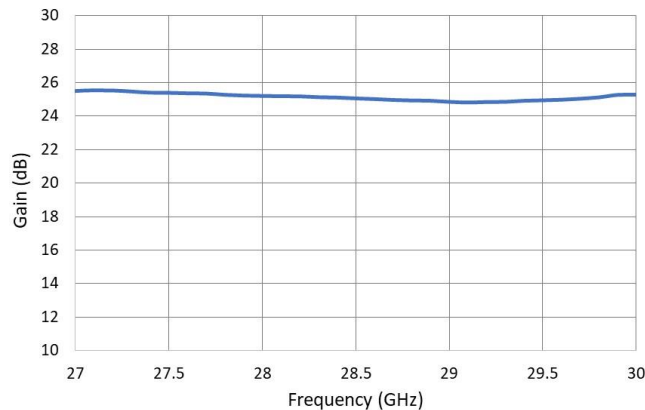
Parameter	Value	Unit
Drain Voltage (Vd)	20 - 28	V
Drain Current (Id1)	up to 264	mA
Drain Current (Id2)	up to 640	mA
Drain Current (Id3)	up to 2112	mA
Gate Voltage (Vg) (Typical Range)	-4	V

Gate voltage will vary based on desired current per stage

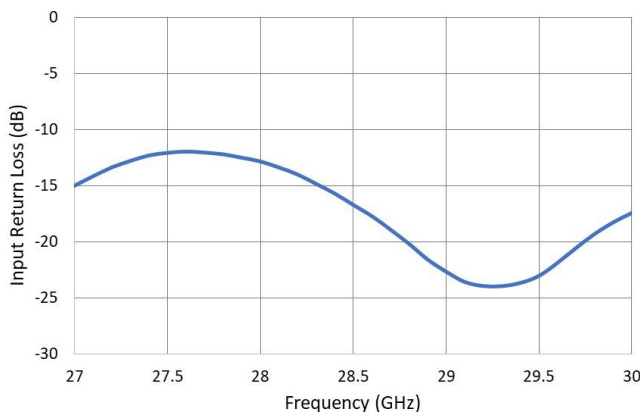
### Small Signal Performance

Test Condition: Vd = 24 V, Idq = 2.0 A, (CW Performance in Fixture, Typical Performance at 25°C)

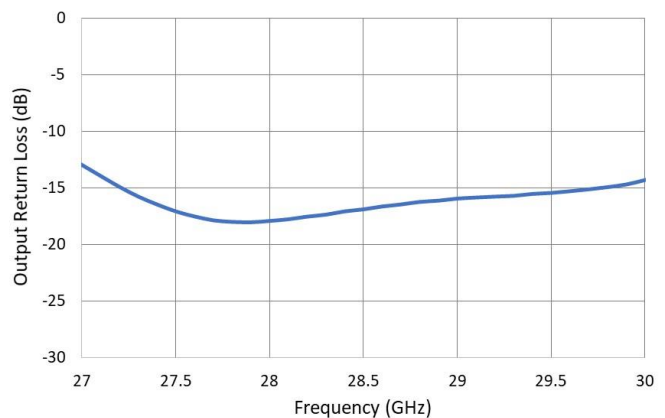
Gain vs. Frequency



Input Return Loss vs. Frequency



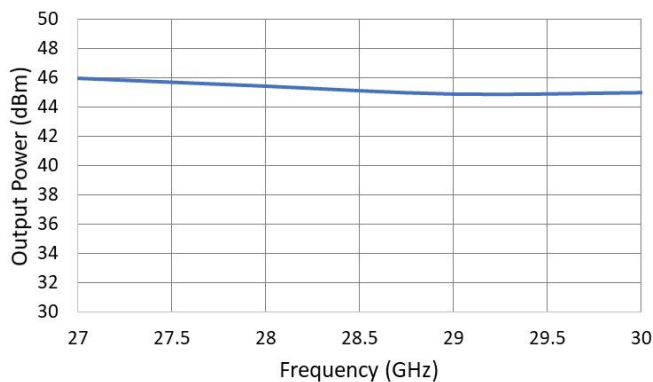
Output Return Loss vs. Frequency



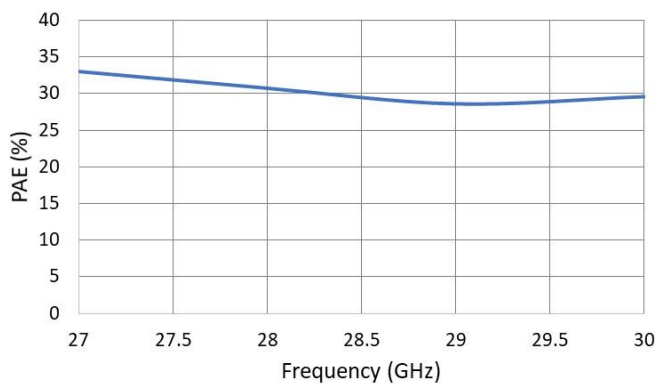
### Large Signal Performance

Test Condition:  $V_d = 24\text{ V}$ ,  $I_{dq} = 2.0\text{ A}$ ,  $P_{in} = 26\text{ dBm}$  ( $P_{sat}$ )  
 (CW Performance in Fixture, Typical Performance at 25°C)

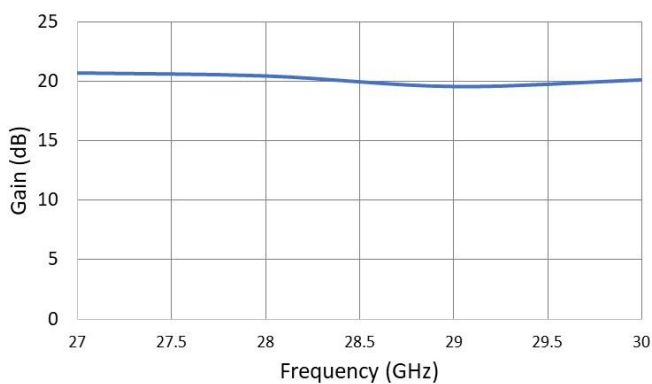
Output Power vs. Frequency (at 26 dBm Pin)



PAE vs. Frequency (at 26 dBm Pin)



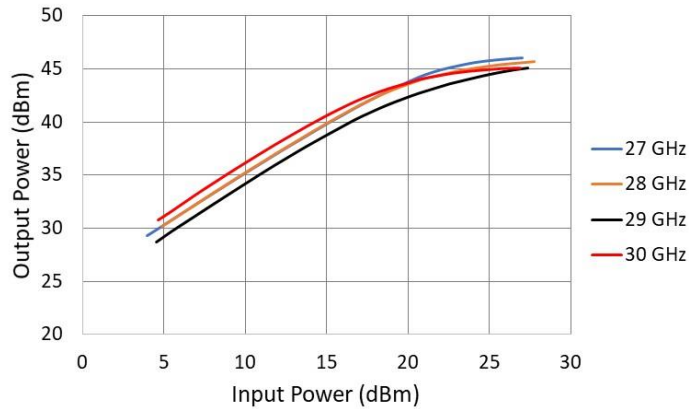
Gain vs. Frequency (at 26 dBm Pin)



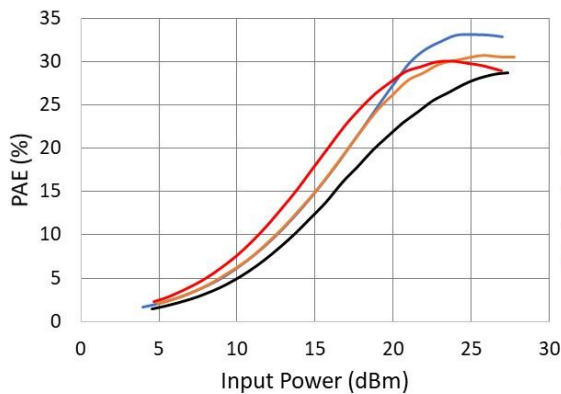
### Large Signal Performance

Test Condition:  $V_d = 24\text{ V}$ ,  $I_{dq} = 2.0\text{ A}$ ,  
(CW Performance in Fixture, Typical Performance at 25°C)

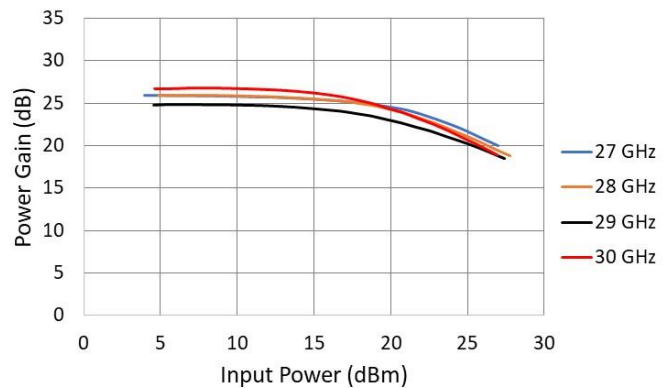
Output Power vs. Input Power vs. Frequency



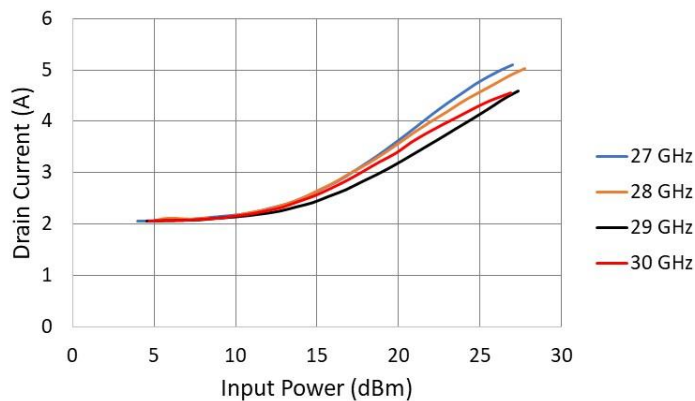
PAE vs. Input Power vs. Frequency



Power Gain vs. Input Power vs. Frequency



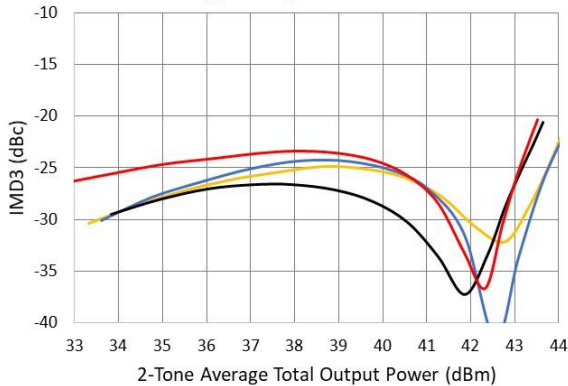
Drain Current vs. Input Power vs. Frequency



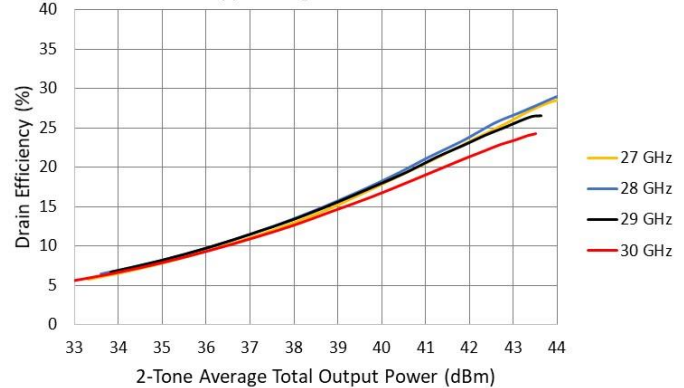
### 2-Tone Linearity Performance

10 MHz Tone Spacing , CW Performance in Fixture, Typical Performance at 25°C,  
Bias as Indicated in Figure

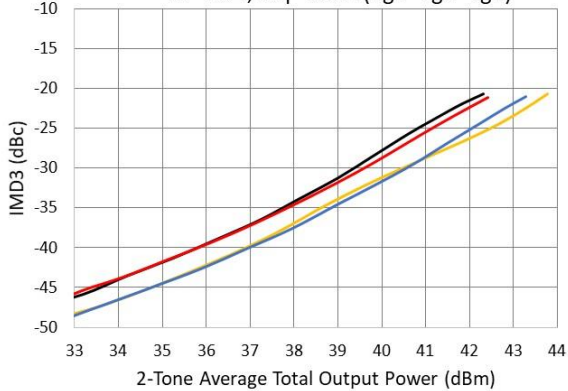
IMD3 vs. 2-Tone Output Power vs. Frequency  
Vd = 26 V, Idq per stage = 0.285, 0.070, 0.860 A



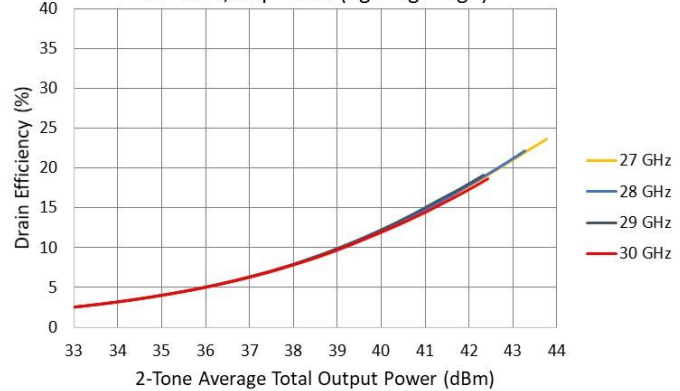
Drain Efficiency vs. 2-Tone Output Power vs. Frequency  
Vd = 26 V, Idq per stage = 0.285, 0.070, 0.860 A



IMD3 vs. 2-Tone Output Power vs. Frequency  
Vd = 26 V, Idq = 3.0 A (Vg1=Vg2=Vg3)



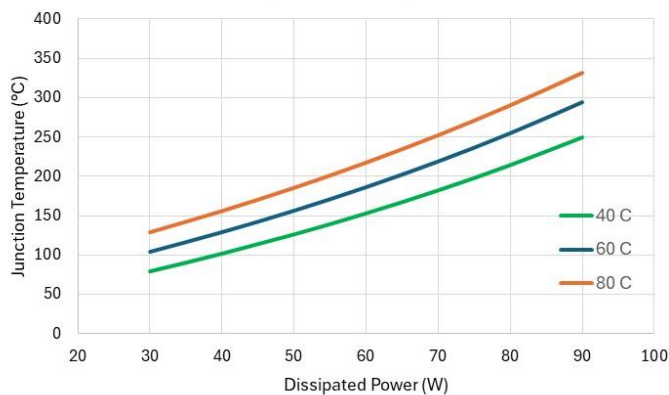
Drain Efficiency vs. 2-Tone Output Power vs. Frequency  
Vd = 26 V, Idq = 3.0 A (Vg1=Vg2=Vg3)



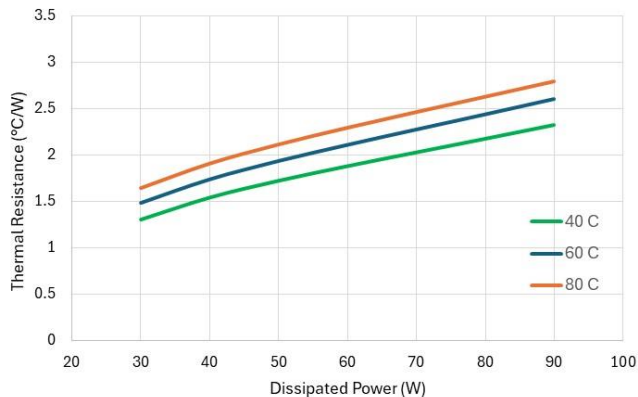
### Thermal Information

#### Junction Temperature and Thermal Resistance Referenced From Backside of Chip

Junction Temperature vs Dissipated Power  
vs. Chip Backside Temperature

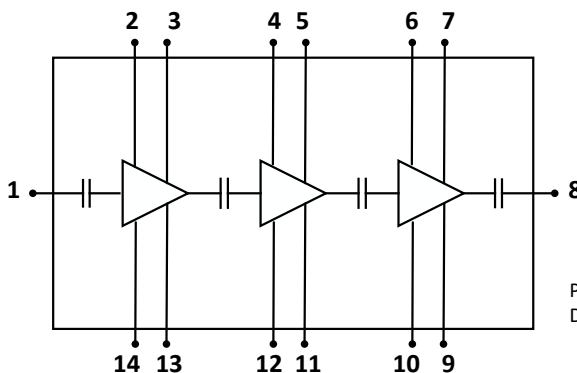


Thermal Resistance vs Dissipated Power



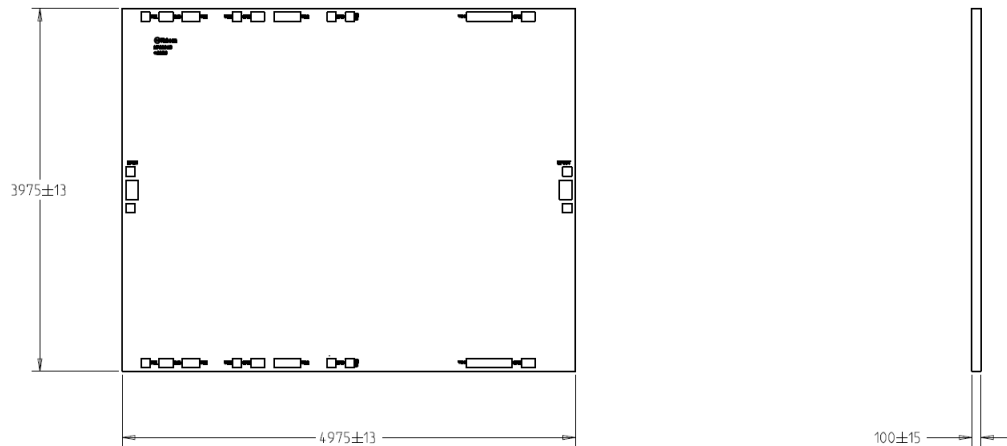
Note 1: Mean time to failure per junction temperature information can be found in the following document:  
[Nxbeam\\_GaN20MMIC\\_Reliability.pdf](#)

### Circuit Block Diagram



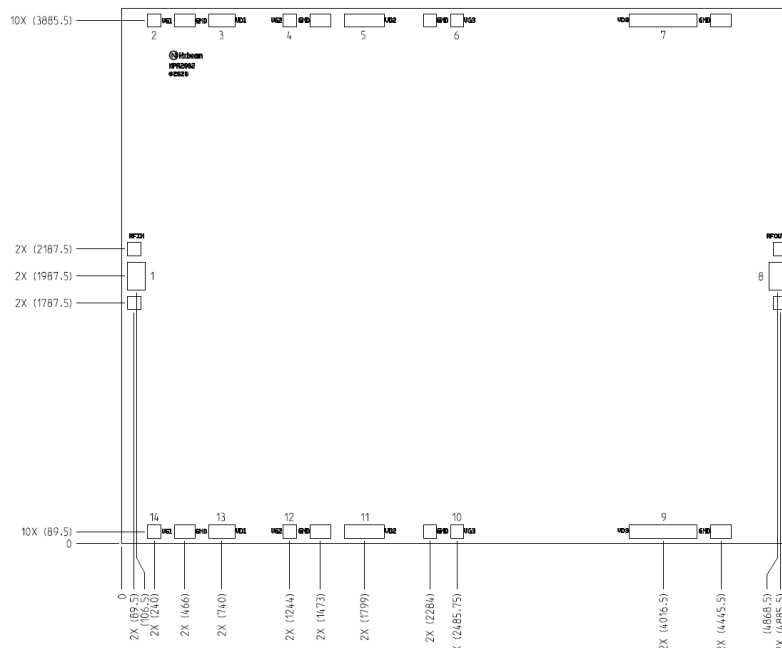
Pin number information detailed under  
Die Size and Bond Pad Information

### Product Dimensions (all dimensions in microns)



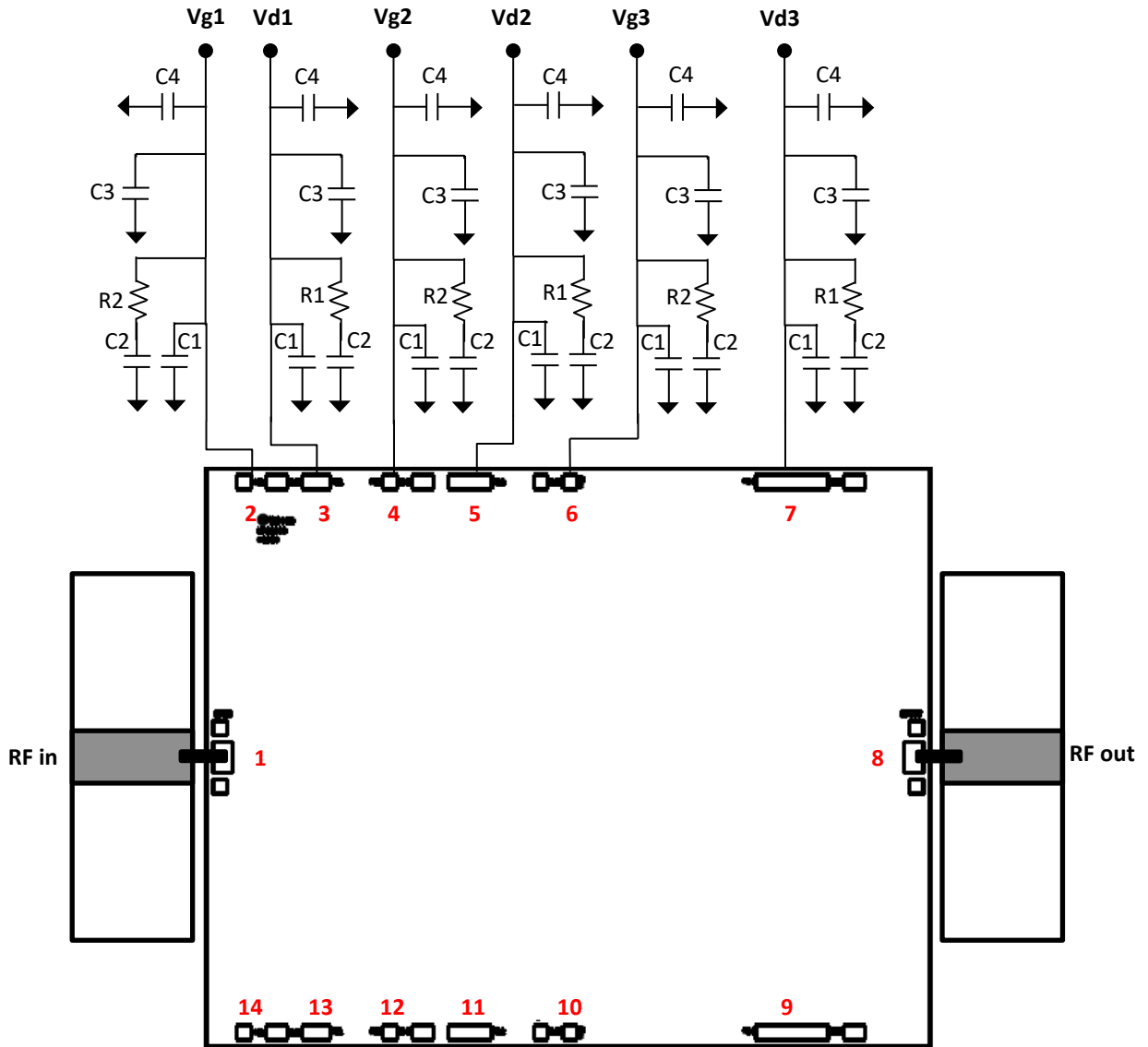
### Die Size and Bond Pad Information

TABLE 1: INTERFACE IDENTIFICATION			
ID	FUNCTION	PAD NUMBER	PAD SIZE
RFIN	RF INPUT	1	134 X 208
RFOUT	RF OUTPUT	8	134 X 208
VG1	GATE VOLTAGE – STAGE 1 (-8V MIN, 0V MAX)	2,14	100 X 100
VD1	DRAIN VOLTAGE – STAGE 1 (0V MIN, 28V MAX)	3,13	196 X 100
VG2	GATE VOLTAGE – STAGE 2 (-8V MIN, 0V MAX)	4,12	100 X 100
VD2	DRAIN VOLTAGE – STAGE 2 (0V MIN, 28V MAX)	5,11	296 X 100
VG3	GATE VOLTAGE – STAGE 3 (-8V MIN, 0V MAX)	6,10	96 X 100
VD3	DRAIN VOLTAGE – STAGE 3 (0V MIN, 28V MAX)	7,9	500 X 100



### Suggested Off-Chip Components

The following diagram shows the recommended off-chip components to be used with the NPA2002-DE. The off-chip components should be duplicated on both top and bottom sides of the chip and located as close to the chip as possible. Bias should be applied to the chip from both sides. Please consult with Nxbeam on other off-chip network variations.



### Recommended Off-Chip Component Values

Capacitor	Value	Resistor	Value
C1	100 pF	R1	1 $\Omega$
C2	0.01 $\mu$ F	R2	10 $\Omega$
C3	1 $\mu$ F		
C4	10 $\mu$ F		



### Assembly Process

- Nxbeam recommends using a silver sintering paste for die attachment of the NPA2002-DE due to their higher thermal conductivities relative to other die attachment methods.
- This product contains metal air bridges so caution should be taken when handling the die to avoid damage.

### Bias Information

#### Bias-up Procedure:

- 1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
- 2.) Ensure power supplies are properly grounded to the product test fixture.
- 3.) Apply a negative gate voltage of -7V to Vg1, Vg2, and Vg3 to ensure all devices are pinched off.
- 4.) Gradually increase the drain bias voltage (Vd1, Vd2, Vd3) to the desired bias level but not to exceed the maximum voltage of 28 V.
- 5.) Gradually increase the gate voltages (Vg1, Vg2, Vg3) while monitoring the drain current until the desired drain current in each stage is achieved.
- 6.) Apply RF signal.

#### Bias-down Procedure:

- 1.) Turn off RF signal.
- 2.) Gradually decrease Vg1, Vg2, and Vg3 down to -7 V.
- 3.) Gradually decrease the drain voltages (Vd1, Vd2, Vd3) down to 0 V.
- 4.) Gradually increase gate voltages (Vg1, Vg2, Vg3) to 0 V.
- 5.) Turn off supply voltages

#### ESD Sensitive Product



### Export Information

This product is controlled by US law for export under the ECCN 3A001.b.2.c. The purchaser of this product, whether in the US or abroad, is responsible for compliance with all US laws regarding export, transfer, or re-transfer of this product. For more information, please refer to the Export Administration Regulations at <https://www.bis.doc.gov/index.php>. Nxbeam reminds you that it is your responsibility to ascertain your export compliance obligations and to comply with all applicable laws and regulations.

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