

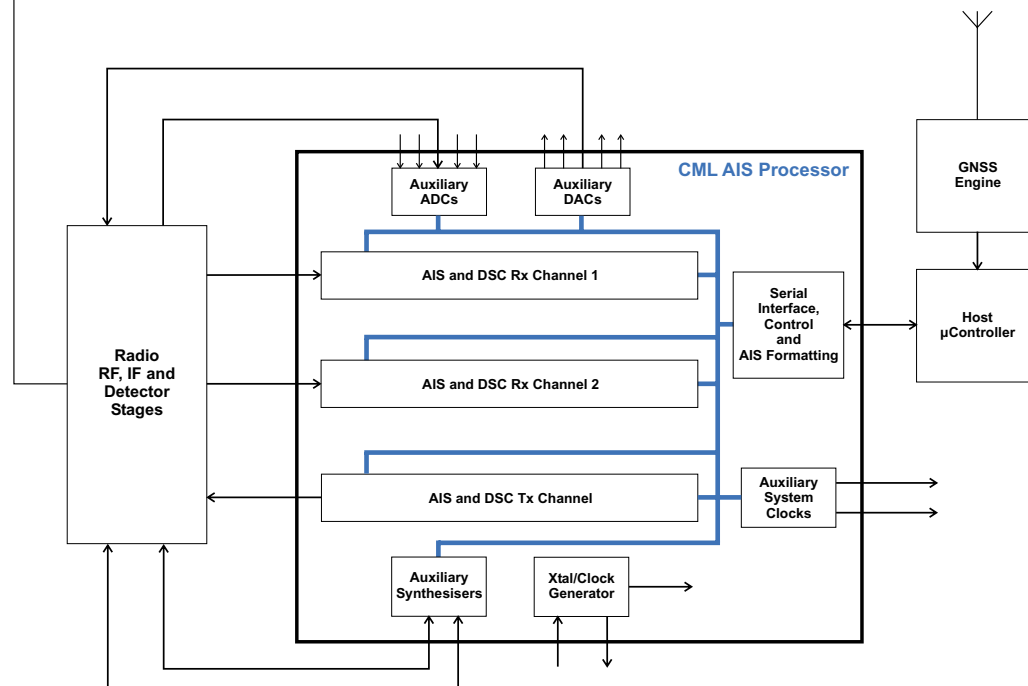
# Marine AIS Processor ICs

## AIS-Dedicated Processors for Maritime Safety

..... for I and Q (Digital) and Limiter-Discriminator (Analogue) Based Systems

### CML AIS Products

With the high integration on-chip of AIS-specific functions and wide-ranging data-signal processing capabilities, these three dedicated AIS IC products will minimise the final-product board-area requirement and component count whilst drastically minimising the system software and processing effort; all with a view to a high-performance, low-cost end-product with greatly accelerated time-to-market.



#### For I and Q based RF Systems

- **CMX910** AIS Class A and B Baseband Processor

#### For Limiter-Discriminator based RF Systems

- **CMX7032** AIS Class B Baseband Processor with RF Synthesisers (FI-1.x)
- **CMX7032** AIS Rx-only Baseband Processor with RF Synthesisers (FI-2.x)
- **CMX7042** AIS Class B Baseband Processor (FI-1.x)

#### With Comprehensive Evaluation and Development Support

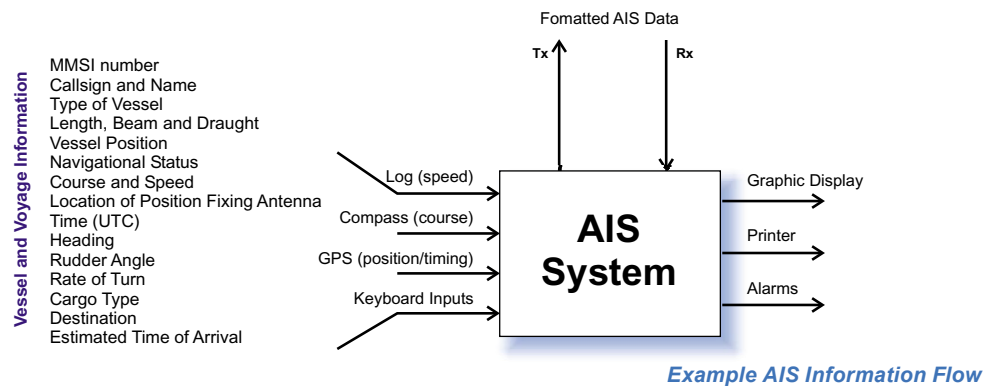
- EV9100, PE0201, PE0401, PE0001 and DE70321

### CML AIS Products for:

- Class A and Class B AIS Equipments
- AIS (Rx Only) Monitors
- AIS Transmit Modules
- Aids to Navigation (AToN)
- Electronic Chart Display and Information Systems (ECDIS)
- AIS Base Stations

# The Marine Automatic Identification System (AIS)

<b>Index . . .</b>		Used extensively as an aid to maritime navigation and safety by ships, aircraft and fixed or floating structures, an AIS transponder continually broadcasts the host vessel's positional and status information. This enables other similarly equipped vessels in the vicinity to receive, decode and display that information, along with information from other navigational systems (radar, GPS, depth recorders), to provide a comprehensive picture of the maritime traffic in the local area.
<b>The AIS System</b>	2	
<b>CML ICs in AIS Systems</b>	3	
<b>CMX910 AIS Class A and B</b>	4	Using an omni-directional broadcast of formatted wireless-data in the VHF maritime band, an AIS system employs two simultaneous Rx channels and a single, frequency-switched, Tx channel.
<b>CMX7032/CMX7042</b>		
<b>FI-1.x AIS Class B</b>	6	The AIS system will normally operate in an autonomous continuous mode. Using Self-Organising Time Division Multiple Access (SOTDMA) technology, AIS messages are packed into over-air time slots that are accurately synchronised using either GNSS or local timing information. An AIS system can handle well over 4,500 reports per minute using individual 26.6ms time slots on both Rx channels.
<b>FI-2.x AIS Rx-only</b>	8	
<b>Evaluation and Support</b>	10	
<b>Device Configuration</b>	back page	Each station transmits and receives over two radio channels to avoid interference problems, and to allow channels to be shifted without communications loss.



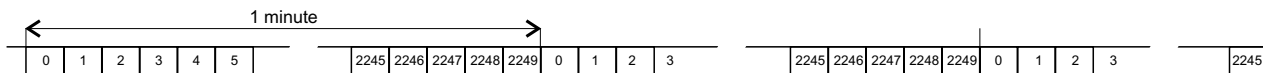
## Self-Organising Time Domain Multiple Access Operation (SOTDMA)

SOTDMA technology is at the heart of the Class A and Class B AIS system's operation.

AIS messages are packed into over-air time slots in a continuous repeating framework.

The timing of each individual slot within the frame is accurately synchronised using either GNSS-based or local timing information.

Each minute in time is divided into 2250 timeslots. Each individual slot carries one vessel's data using HDLC packet protocol formats.



**AIS Slot Timing: 2250 Slots every 60 seconds; Slot length = 26.6ms**

With regard to the slot cycle (described above), the local AIS system transmits the relevant data in HDLC packet format. At the same time it reserves a future slot in the next frame. This timeslot method and the use of two radio channels, avoids, in the long-term, the cumulative effect of packet collisions.

An AIS Class A system will transmit directly in its chosen slot and may use more than one slot period per cycle if required.

An AIS Class B CSTDMA system can only use one slot period and must check its chosen slot for Rx energy before transmitting.

As ships join and leave areas they form local area-networks, taking care not to interfere with each other. As they move out of range of a network, they continue to broadcast their positions, all the time listening for other networks to join.

## The System

- The efficient exchange of navigational data between ships and shore stations
- Autonomous, automatic and continuous operation
- Employs Time Division Multiple Access (TDMA) techniques
- Class A: SOLAS vessels
- Class B: Smaller vessels
- Operates in the VHF maritime mobile band
- Uses two simultaneous AIS channels and one Digital Selcall (DSC) channel
- AIS Modulation: GMSK - 9600bps
- DSC Modulation: FSK - 1200bps
- Transmits:
  - Static and dynamic vessel information
  - Voyage related information
  - Safety messages

## AIS Classes

There are currently two maritime-mobile classes of AIS operation:

### Class A (SOLAS vessels)

- 3 Rx Channels (AIS 1, AIS 2 and DSC) must be monitored simultaneously
- DSC is transmitted as required
- All AIS timing must be sourced from a received GPS (UTC) 'tick' input
- Class A transmissions take priority over Class B
- Class A transmissions may use more than one consecutive slot per cycle

### Class B (Non-SOLAS AIS vessels)

- 2 Rx Channels (AIS 1 and AIS 2) must be monitored simultaneously
- GPS timing is not mandatory - in its absence, timing is obtained from the transmissions of nearby, more accurate AIS transmissions
- Can only use one slot per cycle - gives way to Class A transmissions

- Time Sequence            1 Frame = 1 minute
- 1 Frame                    2250 slots
- 1 Slot                      26.6ms
- AIS Data Rate            9600bps - GMSK

## CML ICs in AIS Systems

AIS IC Product Selector				
- Built on FirmASIC® Technology -				
	CMX910 (Rx/Tx)	CMX7032 (FI-1.x) (Rx/Tx + RF)	CMX7032 (FI-2.x) (Rx-only + RF)	CMX7042 (FI-1.x) (Rx/Tx)
Modulation	GMSK and FSK	GMSK and FSK	GMSK	GMSK and FSK
AIS Support	A and B	B	A and B	B
On-Chip AIS Data Handling Modes	AIS Burst and Raw	AIS Burst and Raw	Processes dual (Rx) channel AIS data to an NMEA data stream output	AIS Burst and Raw
On-chip AIS Data Formatting	HDLC and NRZI	HDLC and NRZI		HDLC and NRZI
AIS Signal Timing	Slot and Sample	Sample	NA	Sample
Peripheral Timing	Sequenced, timed control of external circuits	2 x System Clocks	2 x System Clocks	2 x System Clocks
Rx Modes	AIS and DSC	AIS and DSC	AIS	AIS and DSC
Tx Modes	AIS and DSC	AIS	NA	AIS
RF Channel Bandwidth	12.5 and 25 kHz	25kHz	NA	25kHz
Rx Interface	I and Q	Limiter-Discriminator	Limiter-Discriminator	Limiter-Discriminator
Tx Interface	I and Q	Two-Point Modulation/ I and Q	NA	Two-Point Modulation/ I and Q
Auxiliary ADCs and DACs	5 x 10-bit (Mux) ADCs 5 x 10-bit DACs	4 x 10-bit (Mux) ADCs 4 x 10-bit DACs	NA	4 x 10-bit (Mux) ADCs 4 x 10-bit DACs
Auxiliary System Clocks	None	2 x System Clocks	2 x System Clocks	2 x System Clocks
RF Synthesisers	None	2 x Individual (100 to 600 MHz)	2 x Individual (100 to 600 MHz)	None
Control Interface	C-BUS and Expansion Port	C-BUS	RS232	C-BUS
AIS Tx System Format Compatibility	SOTDMA CSTDMA	SOTDMA CSTDMA	NA	SOTDMA CSTDMA
Device Configuration via:	Configuration File	Function Image™	Function Image™	Function Image™
Supply Requirements	3.0 to 3.6 V			
Packages	64-lead LQFP (L9) 64-no lead VQFN (Q1)	64-lead LQFP (L9) 64-no lead VQFN (Q1)	64-lead LQFP (L9) 64-no lead VQFN (Q1)	48-lead LQFP (L4) 48-lead VQFN (Q3)
Evaluation	EV9100 EvKit	PE0201 EvKit PE0001 Interface Card DE70321 DemoKit	PE0201 EvKit DE70321 DemoKit	PE0401 EvKit PE0001 Interface Card

Designed for implementation in both the simple, traditional, limiter-discriminator and the more versatile digital (I and Q) based AIS systems, CML currently offers three flexible AIS compatible ICs:

**CMX910** AIS Baseband Processor for I and Q based Systems

**CMX7032** AIS Data Processor with RF Synthesiser for Limiter-Discriminator based systems (FI-1.x), **or**

AIS Rx-only Data Processor with RF Synthesiser for Limiter-Discriminator based systems (FI-2.x)

**CMX7042** AIS Data Processor for Limiter-Discriminator based systems (FI-1.x)

### AIS Transponders

Feature-rich, each offers two simultaneous Rx channels and one Tx channel, a channel which can be frequency-switched in line with AIS regulations.

High on-chip integration with AIS and DSC specific data manipulation and frame-formatting allows the ICs to handle the majority of the computationally intensive tasks normally carried out by the host.

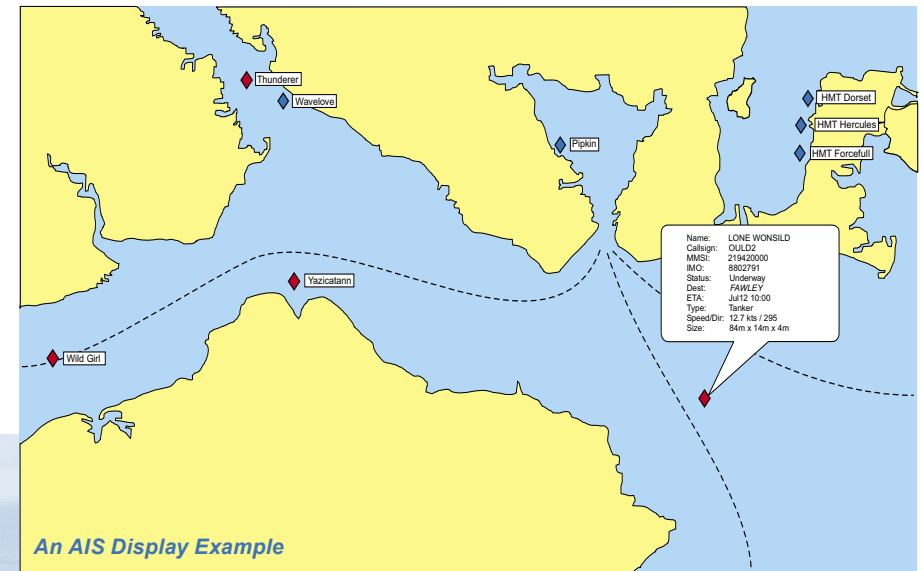
Using a serial data/command interface (C-BUS) these products use a simple transaction-oriented command/response protocol to address specific registers within the IC, with data buffering on chip.

Accurate timing, obtained from a GNSS source, is maintained to provide both AIS related and system timings.

In addition to AIS signal and data handling, these products offer a range of auxiliary functions for peripheral communications, including ADCs, DACs and synthesised system clocks.

### AIS Rx Only

New to the product roadmap is the AIS Rx-only configuration of the CMX7032 using FI-2.x. Designed to operate virtually stand-alone, this configuration requires no host control.



# CMX910 AIS Baseband Processor for I and Q based Systems

Designed specifically for all current modes of AIS operation, the **CMX910** offers a highly integrated IC capable of performing all of the required data-handling, formatting, timing, distribution and control functions under the control of the host.

Provided on-chip are both of the mandated GMSK Rx channels and a single Tx channel. Selectable to 12.5 and 25 kHz channel modes for AIS, the **CMX910** accommodates, in Rx and Tx, both full AIS data packet assembly and disassembly and a basic 'raw' data facility. Both AIS (GMSK) and DSC (FSK) I and Q modulated signalling modes are available. A third, parallel (Rx) decode path, accommodates the DSC (FSK) signalling from an external modem for Class A AIS applications.

Integration of all AIS functions, including versatile synchronisation and slot and sample timing and control facilities is available. Control and interfacing, including upgraded 'data-streaming', are via the C-BUS serial interface, with a host-controlled expansion port for the addition of an external FX/MX604 modem IC.

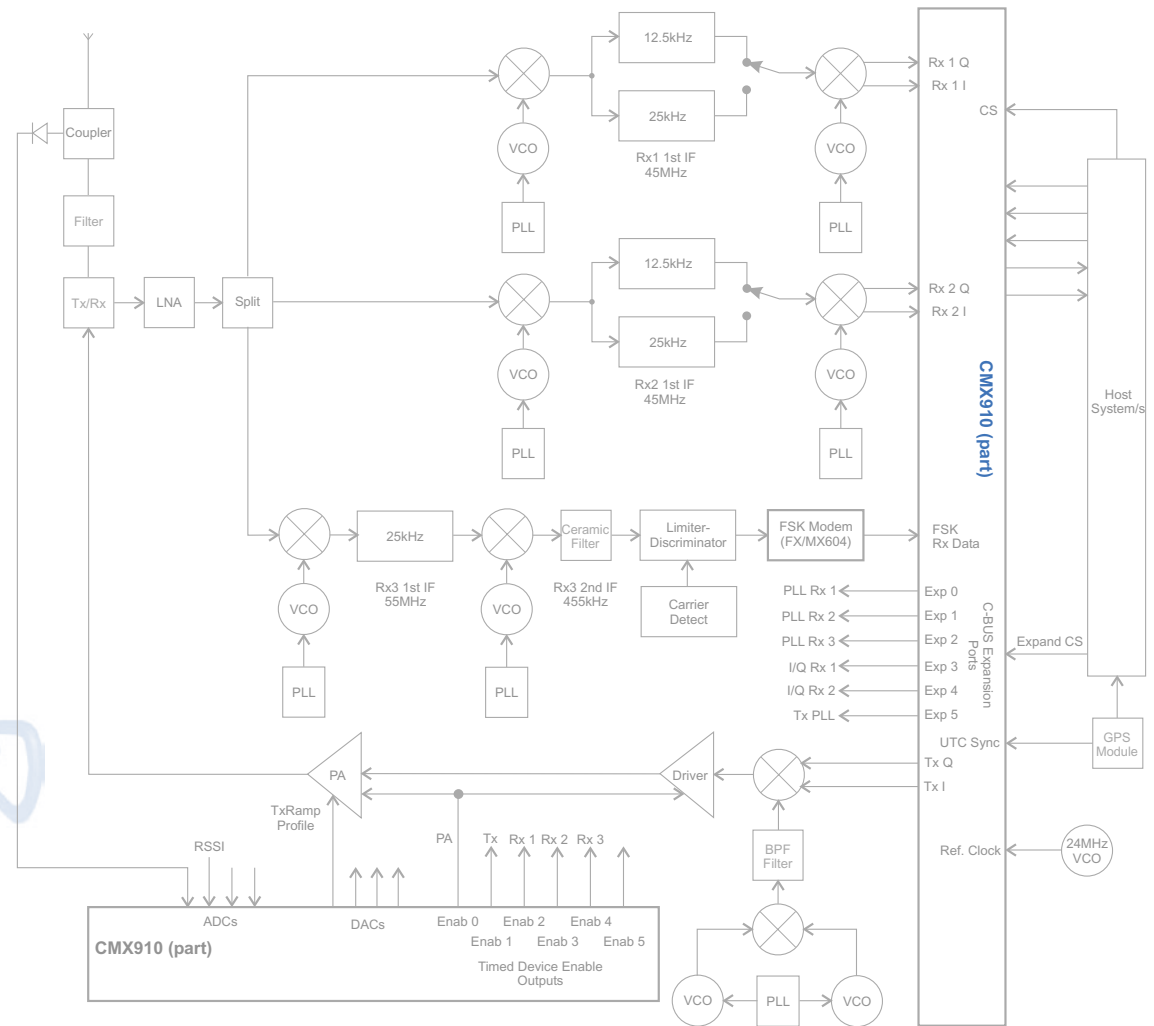
The provision of the C-BUS expansion port, an RF device enabling port and a number of auxiliary uncommitted ADCs and DACs, simplifies the system hardware implementation, further reducing the overall equipment cost and size. One of the on-chip DACs has an additional, programmable (RAMDAC) ramp-mode (up or down) feature which is particularly useful for controlling the output profile of the transmitter-power at the beginning and end of a transmit slot to prevent interference to other users by controlling the power-profile of the radio's PA. Similarly, a bank of multiplexed analogue-to-digital converters provides monitor facilities to the IC and to the system.

## Rx and Tx On-Chip Signal Paths

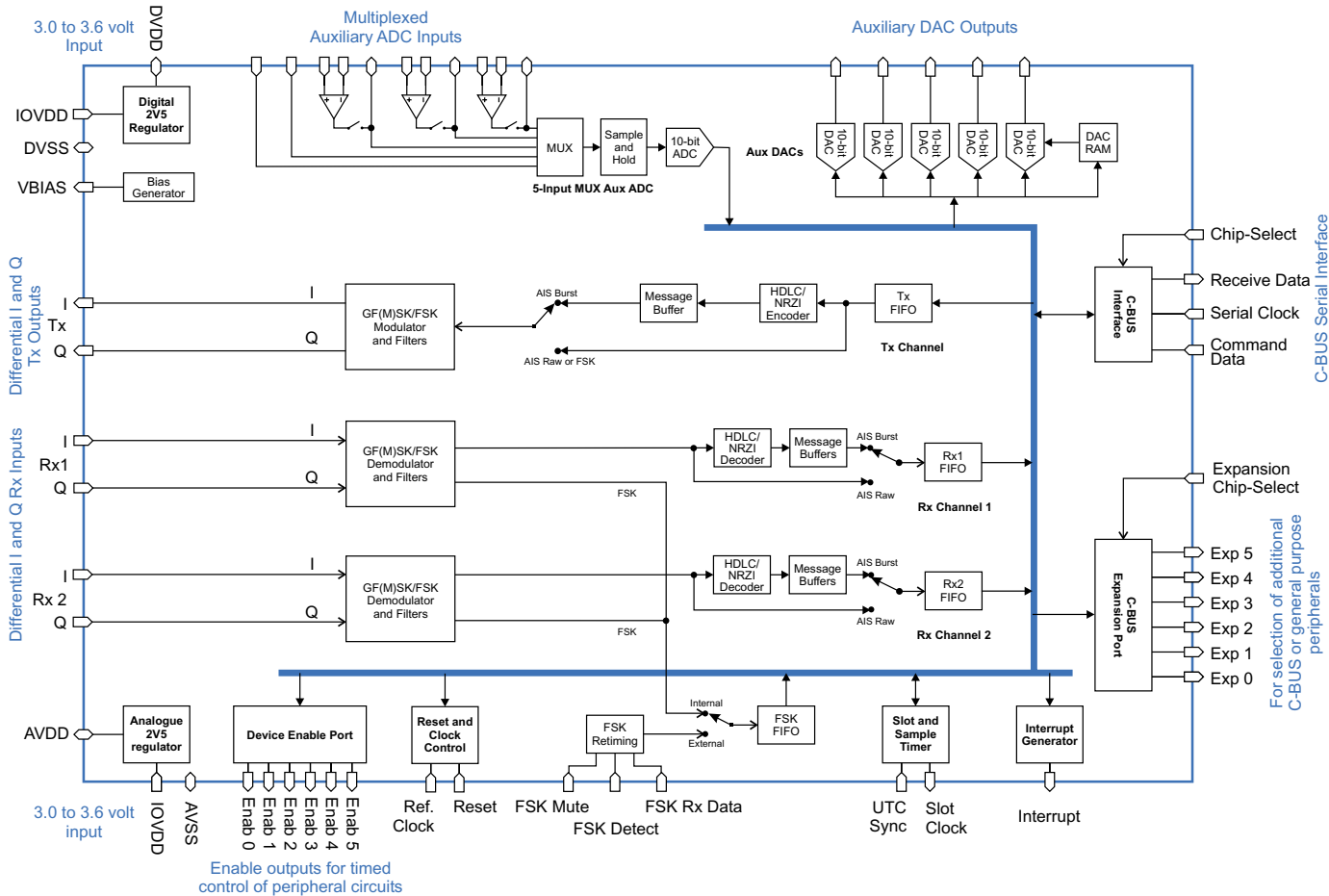
- Simultaneous Reception
  - Two AIS or One AIS, One DSC
- Differential I and Q Signalling
- Two Parallel I and Q Rx Paths
- One I and Q Tx Path
- Additional FSK (DSC) Decode Path
  - 1200bps Demodulator Interface
- Channel Filtering

## AIS Data Handling

- NRZI Coding
- HDLC Processing
  - System Flags
  - Training Sequence
  - Bit-Stuffing
- AIS and Raw Data Modes
- CRC Generation and Checking
- Supports Carrier Sensing (CSTDMA) Operations
- Integrated Rx and Tx Buffers
- Flexible Sample and Slot Timing from GNSS-Based (UTC) Source



CMX910 Peripheral Operations



CMX910 Functional Diagram

### Auxiliary Functions

- C-BUS Expansion Port
  - Select and Address Peripheral C-BUS (SPI) ICs
- External (RF) Device Enable Port
  - The Timed Operation of Peripheral System Functions
- Multiplexed Auxiliary ADC Inputs
  - External System Signal Monitoring (RSSI, Temperature, RF Power, Battery Voltage)
- Auxiliary DAC Outputs
  - External System Control
  - RAM DAC Tx Power Profiling

### Power and Control

- 3.0 to 3.6 Volt Low-Power Requirement
- Serial Data/Command Interface with On-Chip Registers
- Raw and Formatted AIS Data Handling
- Full AIS Data Formatting (HDLC and NRZI coding)
- AIS Sample Timing On-Chip

### Features

- Half-Duplex GMSK, FSK and DSC capabilities
- Flexible signal channels
  - Two simultaneous Rx
  - One Tx
  - Optional-FSK interface
- Supplementary Rx DSC-only data path for external FSK demodulator
- AIS formatted data and raw data modes
- Slot/Sample counter with UTC timing interface
- I and Q (Tx and Rx) radio interface
- High performance GMSK encoding/decoding
- Supports Carrier-Sensing Channel Access (CSTDMA) operation
- Supports Self Organising Time Domain Multiple Access (SOTDMA) operations
- Auxiliary ADC and DAC functions
  - 5 (10-bit) DACs
  - 5-Input MUX (10-bit) ADC
- C-BUS (SPI compatible) serial control interface with expansion port
- RF device-enable facilities
- Message progress-reports to host
- Optimum co-channel and adjacent-channel performance
- Low-power (3.0 to 3.6 V) operation with 'Sleep' and 'Dynamic' powersave
- EV9100 EvKit support for evaluation, experimentation and design-in
- Compact package styles

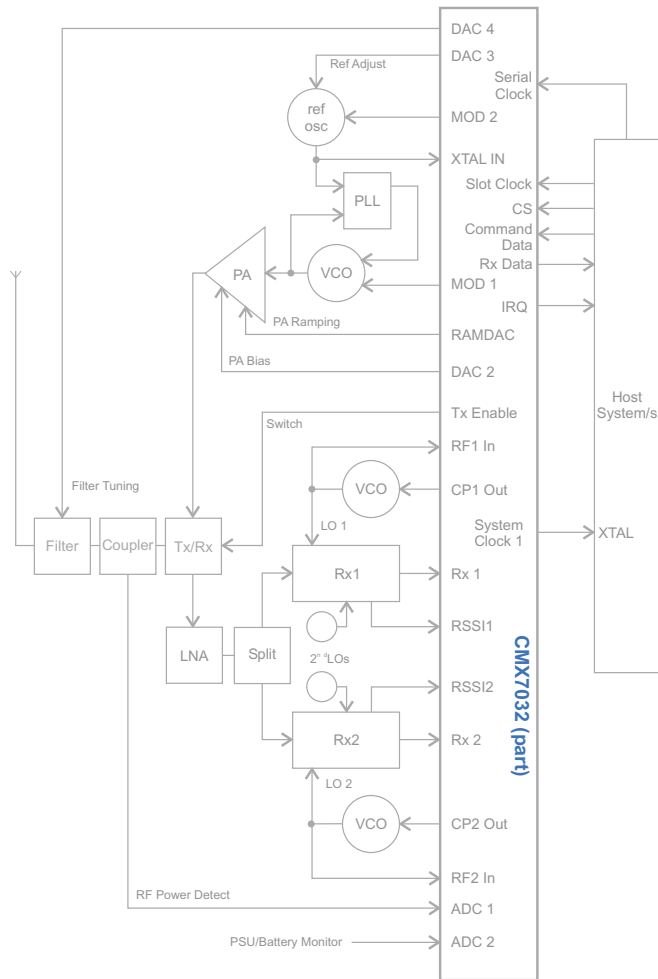
### Package Styles

- CMX910L9 64 Lead LQFP
- CMX910Q1 64 No-Leads VQFN



# CMX7032 AIS Class B Baseband Processor with RF Synthesisers (FI-1.x)

## CMX7042 AIS Class B Baseband Processor (FI-1.x)



CMX7032 (FI-1.x) Peripheral Operations

Two highly integrated data signalling processor ICs, both of which fulfil the requirements of the Class B marine Automatic Identification System (AIS) transponder market.

Comprising two parallel limiter-discriminator Rx paths and one I and Q or two-point modulation Tx path, these ICs are half-duplex in operation. The Rx paths are configurable to AIS or DSC operation, the Tx path is configurable to AIS only. Both products provide AIS (Rx/Tx) raw and formatted data processes and DSC Rx raw and de-formatted data.

Provision of a number of auxiliary ADCs and DACs, two auxiliary system clocks and integrated Rx/Tx data buffers further simplify the system hardware design.

Both products are identical in functionality, with the exception that the CMX7032 provides two on-chip RF synthesisers and the CMX7042 none, which enables it to be supplied in a smaller, more compact package.

These devices are built on CML's proprietary FirmASIC® component technology. On-chip sub-systems are configured by a Function Image™: a data file that is uploaded during device initialisation and which defines the device's function and feature set. The Function Image™ can be loaded automatically from an external EEPROM or from the host µController over the C-BUS serial interface. The device's functions and features can be enhanced or altered by subsequent Function Image™ releases, facilitating in-field upgrades.

### Rx and Tx On-Chip Signal Paths

- Simultaneous Reception
  - Two Parallel AIS Paths
- Limiter-Discriminator Rx Interfaces
- One I and Q or Two-Point Modulation Tx Output

### AIS Data Handling

- NRSI Coding
  - System Flags
  - Training Sequence
  - Bit-Stuffing
- AIS Formatted and Raw Data Modes
- CRC Generation and Checking
- Supports Carrier Sensing (CSTDMA) Operations
- Integrated Rx and Tx Buffers
- Sample Counter Timing from GNSS-Based (UTC) Source

### Rx DSC Operations

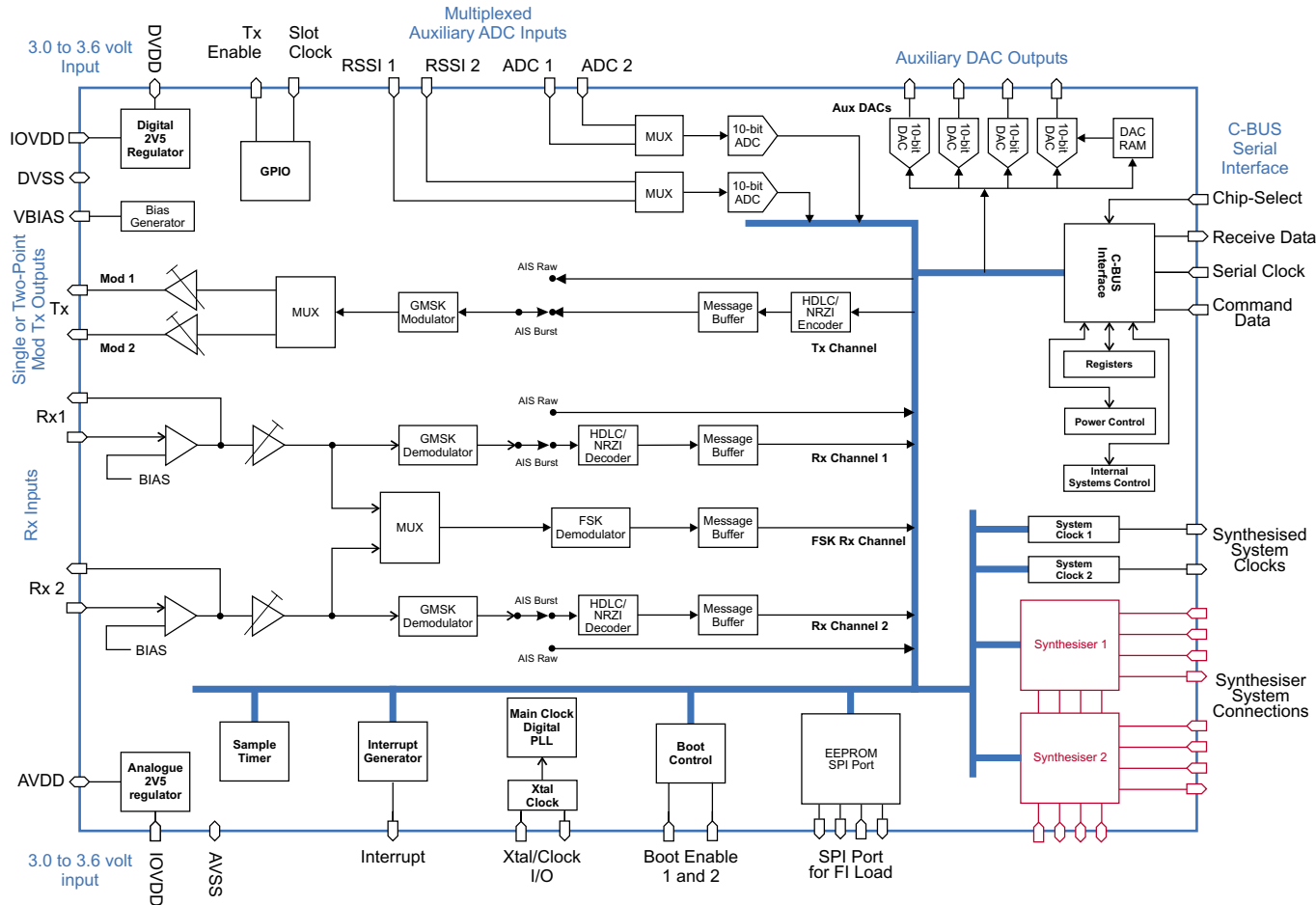
- Rx1 or Rx2 Channels Available for Rx DSC operation
- Raw or Formatted Modes
- 6db/octave De-emphasis Rx Filter
- 1200 Baud FSK Data
- Raw Mode:
  - 16-bit Words Directly to µC
- De-formatted:
  - Dot Pattern and Phasing Detection
  - Decoded Character and Error Bits to µC

### Auxiliary Functions

- Multiplexed Auxiliary ADC Inputs
  - External System Signal Monitoring (RSSI, Temperature, RF Power, Battery Voltage)
- Auxiliary DAC Outputs
  - External System Control
  - RAMDAC Tx Power Profiling
- Synthesised System Clocks
- RF Synthesisers (CMX7032)

### Power and Control

- 3.0 to 3.6 Volt Low-Power Requirement
- Serial Data/Command Interface with On-Chip Registers
- Raw and Formatted AIS Data Handling
- Full AIS Data Formatting (HDLC and NRSI coding)
- AIS Sample Timing On-Chip



CMX7032 and CMX7042 (FI-1.x Configured) Functional Diagram

## Features

- Built on FirmASIC® technology
- Half-duplex GMSK and FSK capabilities
- Flexible signal channels
  - Two simultaneous Rx
  - One Tx
- AIS 25kHz channel
  - 9.6kbps GMSK with a BT of 0.4 and a modulation index of 0.5
- Rx DSC
  - 1200Baud FSK with frequency modulation (1300Hz - 2100Hz) around a 1700Hz sub-carrier
- Rx/Tx AIS formatted data and raw data modes
- Rx DSC de-formatted data and raw data modes
- Sample Counter/Timer
- Limiter-Discriminator Rx interface
- Selectable I and Q or Two-Point Modulation Tx outputs
- Two auxiliary synthesised system clocks
- Two independent RF synthesisers (CMX7032)
- Configuration by Function Image™ file upload
- High performance GMSK encoding/decoding
- Supports Carrier-Sensing Channel Access (CSTDMA) Operation
- Supports Self Organising Time Domain Multiple Access (SOTDMA) operation
- C-BUS serial control interface
- Auxiliary ADC and DAC functions
  - 4 (10-bit) DACs
  - 2 x 2-Input MUX (10-bit) ADCs
- Message progress-reports to host
- Optimum co-channel and adjacent-channel performance
- Low-power (3.0 to 3.6 V) operation with 'Sleep' and 'Dynamic' powersave
- PE0001, PE0201 and PE0401 support for evaluation, experimentation and design-in
- Compact package styles

## Package Styles

- CMX7032L9 64 Lead LQFP
- CMX7032Q1 64 No-Leads VQFN
- CMX7042L4 48 Lead LQFP
- CMX7042Q3 48 No-Leads VQFN

# FI-1.x

## Series Variants

This block diagram illustrates the functions available from the CMX7032 and CMX7042 ICs using Function Image™ 1.x. Functions in black are common to both products; functions in red on the diagram are specific to the CMX7032.

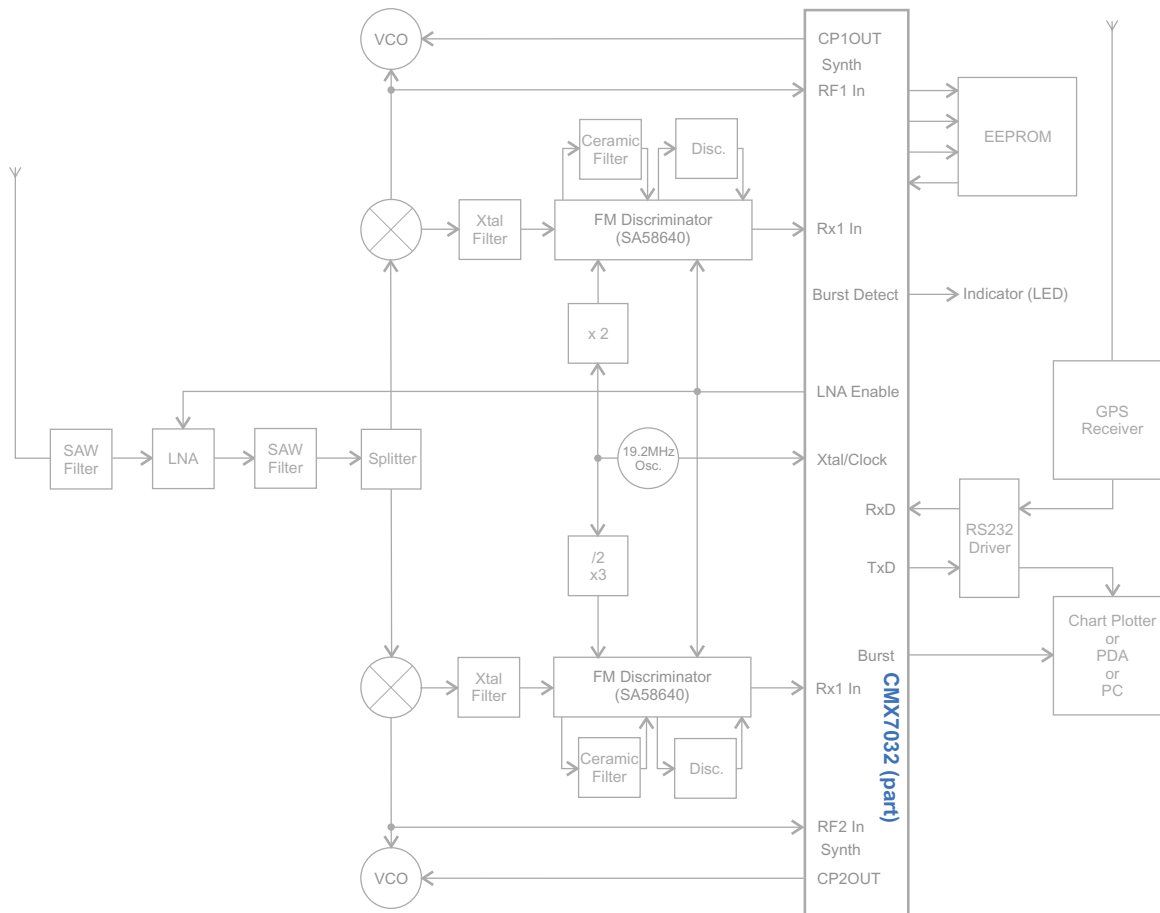


# CMX7032 AIS Rx-only Baseband Processor with RF Synthesisers (FI-2.x)

Configured by the AIS Rx-only Function Image™ (FI-2.x), the CMX7032 offers the core of a simple Automatic Identification System receiver. With its two separate on-chip GMSK-based receiver channels interfaced to a limiter-discriminator driven RF system, the CMX7032 will automatically demodulate and decode incoming baseband AIS signals, providing them separately at the Tx Data output as NMEA 0183 HS formatted data.

Further peripheral support is provided by the IC's dual RF synthesisers and programmable clock generators. A dedicated enabling output is available to the system LNA control function. In addition, to enable a complete local-surface picture, provision is made to handle GPS data via the Rx Data input; processes are allocated to pass-through the (GPS) positional data when the IC is not busy with the AIS signal processing.

Designed for stand-alone operation, this IC requires no host micro-controller: the configuration Function Image™ is loaded from a peripheral EEPROM. Provision is made to allow user configuration of the EEPROM contents prior to loading to the memory.



CMX7032 (FI-2.x) Rx-only Peripheral Operations

## Rx and Tx On-Chip Signal Paths

- Simultaneous Reception on Two AIS Channels
- Dual GMSK Demodulators
- Fixed Modulation Format Compatibility:
  - AIS 25kHz Channels
  - GMSK: 9600bps, BT = 0.4, 2.4kHz Deviation
- Gain-adjustable Matching and Input Stages

## Power and Control

- 3.0 to 3.6 Volt Low-Power Requirement
  - RFV<sub>DD</sub>: 2.25 to 2.7 Volts
- Full AIS Rx Data handling (HDLC and NRSI Decoding)
- Host-less Control:
  - Function Image™ (2.x) loaded from System EEPROM
  - User Configuration Options on Memory Contents
- GPS Pass-through Facility via Rx Data Input

## Auxiliary Functions

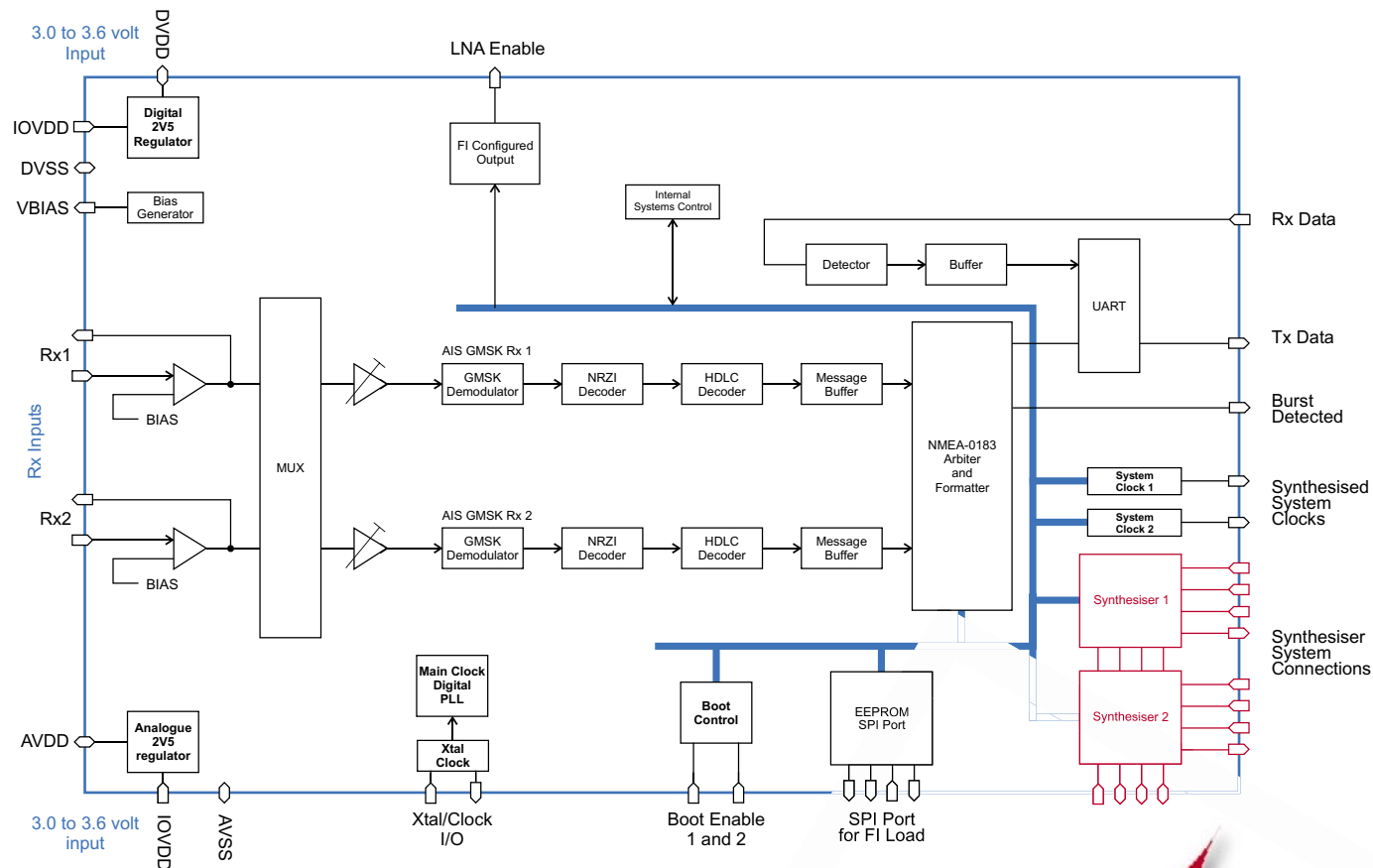
- External LNA Enable Port
- Two Integer-N RF Synthesisers
  - Minimal Reference Spurs for Low Phase-Noise
  - Charge Pump: High/Low Soft Selectable Current Setting
  - Nominal Current is User Defined
- Synthesised System Clocks
- 'Valid AIS Burst Received' Output (LED)

## AIS Data Handling

- AIS Burst Mode with Full AIS Frame Formatting
  - NRSI Decoding
  - HDLC Processing
  - Training Sequence
  - System Flags
  - Bit De-stuffing
- AIS and Raw Data Modes
- CRC Checking
- Supports Carrier Sensing (CSTDMA) Operations
- Four 160 Byte Rx Data Buffers
  - Automatic Storage of 4 x 5-Slot AIS Bursts (Two Per Channel)



# CMX7032 AIS Rx-only Processor



CMX7032 (FI-2.x Configured) Rx-only Functional Diagram

## Features

- Built on FirmASIC® technology
- AIS Rx-only
- Dual GMSK demodulators
- AIS data output in RS232 - NMEA 0183 HS format *National Marine Electronics Association (NMEA)*
- Optimum Rx co-channel performance
- Configurable by Function Image™ (FI-2.x)
- Automatic FI loading from EEPROM for host-less operation
- FI configured output for LNA operation
- Two RF synthesisers
- Two auxiliary system clock generators
- Limiter-Discriminator Rx interface
- PE0201 EvKit and DE70321 DemoKit support for evaluation, experimentation and development design-in
- Compact package styles

## Package Styles

- CMX7032L9 64 Lead LQFP
- CMX7032Q1 64 No-Leads VQFN

# FI-2.x

**New**  
**AIS Rx-only**  
**Function Image™**  
**FI-2.x**



## Evaluation and Demonstration Support

To facilitate evaluation and experimentation, and to reduce design time, the following pcb-based products are available for the evaluation of these AIS ICs:

- **CMX910** [EV9100](#) Evaluation Kit
- **CMX7032** [PE0201](#) Evaluation Kit and [PE0001](#) Evaluation Kit Interface Card
- **CMX7042** [PE0401](#) Evaluation Kit and [PE0001](#) Evaluation Kit Interface Card
- **CMX7032** [DE70321](#) AIS Rx/Tx and Rx-only Demonstration and Development Kit (offers downloadable design-support files)



### EV9100 Evaluation Kit

The EV9100 EvKit is available for the evaluation, experimentation and design-in of the CMX910 AIS Baseband Processor IC. Comprising a digital/analogue pcb with an on-board CMX910 device, the evkit provides access to the CMX910's baseband signal, control and data interfaces as well as its auxiliary ADC and DAC functions.

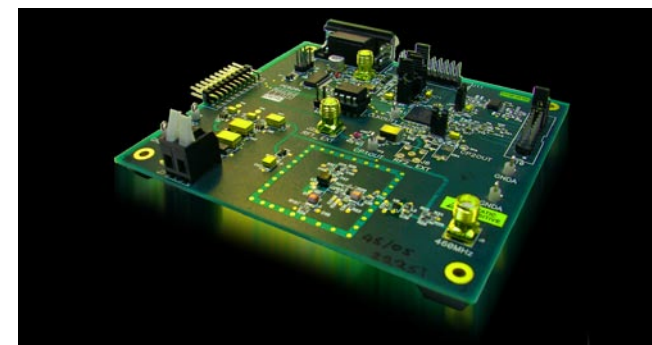
The evkit also provides an FX604 FSK modem and associated circuitry to allow evaluation of the CMX910's external FSK interface.

- Target CMX910 IC On Board
- Auxiliary ADC and DAC Interface
- Digital/Analogue PCB with Low Noise Floor
- Differential and Single-ended Baseband Interface
- FX604 modem IC fitted for Additional (DSC) Rx Channel
- C-BUS Serial Control and Data Interface
- 19.2MHz Device Clock
- On-board Access to all CMX910 Signals, Commands and Data
- Interfaces to RF Daughter-board with all Necessary Signals
- On-board Power Regulation and Distribution

### PE0201 Evaluation Kit

The PE0201 Evaluation Kit is designed to assist in the evaluation and application development of the CMX703x range of *FirmASIC*® products, in this case, the CMX7032. In the form of a populated PCB the PE0201 comprises a target IC, appropriate supporting components and circuitry, including an on-board 460MHz VCO operating in conjunction with one of the IC's on-chip synthesisers.

- Target CMX703x IC On Board
- Evaluates Both RF and Baseband Capabilities
- On-Board 460MHz VCO
- Command and Control by PC via the PE0001 EvKit Interface Card or by User's own  $\mu$ C Development Application or Environment
- Socketed EEPROM Option for Function Image™ Operations
- In-circuit Serial Flash Programming
- On-board Access to all CMX703x Signals, Commands and Data
- On-board Regulators Operate from a Single 5 Volt Supply





#### PE0401 Evaluation Kit

The PE0401 Evaluation Kit is designed to assist in the evaluation and application development of the CMX704x range of *FirmASIC*<sup>®</sup> products, in this case, the CMX7042. In the form of a populated PCB the PE0401 comprises a target IC complete with appropriate supporting components and circuitry.

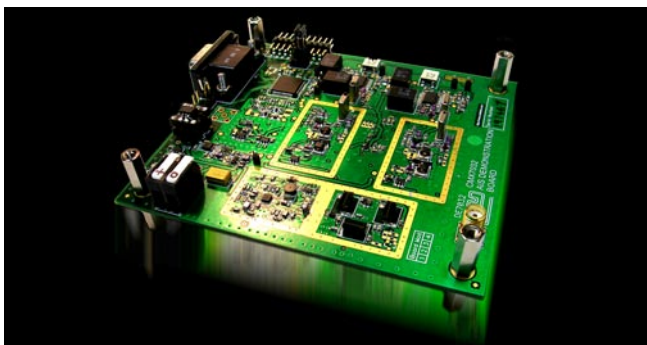
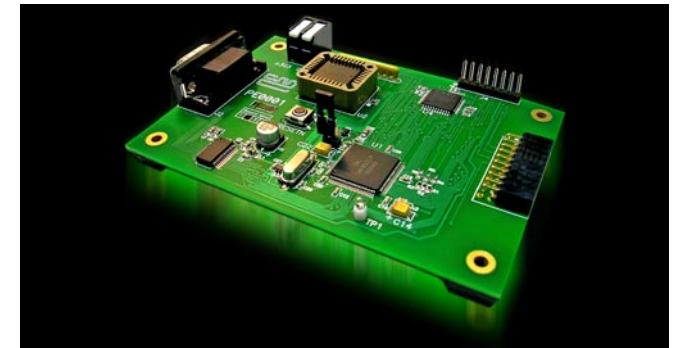
- Target CMX704x IC On Board
- Command and Control by PC via the PE0001 EvKit Interface Card or by User's own  $\mu$ C Development Application or Environment
- Socketed EEPROM Option for Function Image™ Operations
- In-circuit Serial Flash Programming
- On-board Access to all CMX703x Signals, Commands and Data
- On-board Regulators Operate from a Single 5 Volt Supply

#### PE0001 Evaluation Kit Interface Card

The PE0001 EvKit Interface Card is a global interface system for use with evaluation kits for CML's new generation ICs, including products based on *FirmASIC*<sup>®</sup> technology.

Supplied with a PC GUI, and in the form of a populated PCB, the PE0001 provides a graphical way of addressing all of the relevant EvKit's target ICs via the C-BUS interface.

- Global Interface Card for CML's New Generation IC Evaluation Kits
- C-BUS Read, Write and Reset Operations to Target IC
- 8051  $\mu$ Controller Based Operation
- Physical Mating Interface for Wide Range of Target EvKit Boards
- Power Drawn from Target EvKit or Standalone
- PC GUI, Firmware and Hardware Provided  
- Updates available from CML website
- Function Image™ Handling for *FirmASIC*<sup>®</sup>-based Projects
- 4Mbit of Re-programmable Flash Memory
- PC Control and Communications via RS232 Interface



#### DE70321 AIS Demonstration, Evaluation and Development Kit

The DE70321 DemoKit is a complete AIS Class B (IEC 62287) technology demonstrator aimed at speeding manufacturers' design and development of AIS Class B transponders and AIS receiver products using the CMX7032 AIS Class B Baseband Processor with RF Synthesiser IC. This compact PCB-based product measures 100mm x 112.5mm.

This design is a flexible platform to allow users to configure and evaluate with two build options:

- Class B Transceiver (using CMX7032 FI-1.x)
- Dual Channel Rx-only (using CMX7032 FI-2.x)
- Shipped Pre-loaded with FI-2.x - Dual Rx-only Demonstrator

Further Design Support is available from the My CML Technical Portal:

- A Complete Bill of Materials (BOM)
- Layout Schematics
- Design Files

## Device Configuration

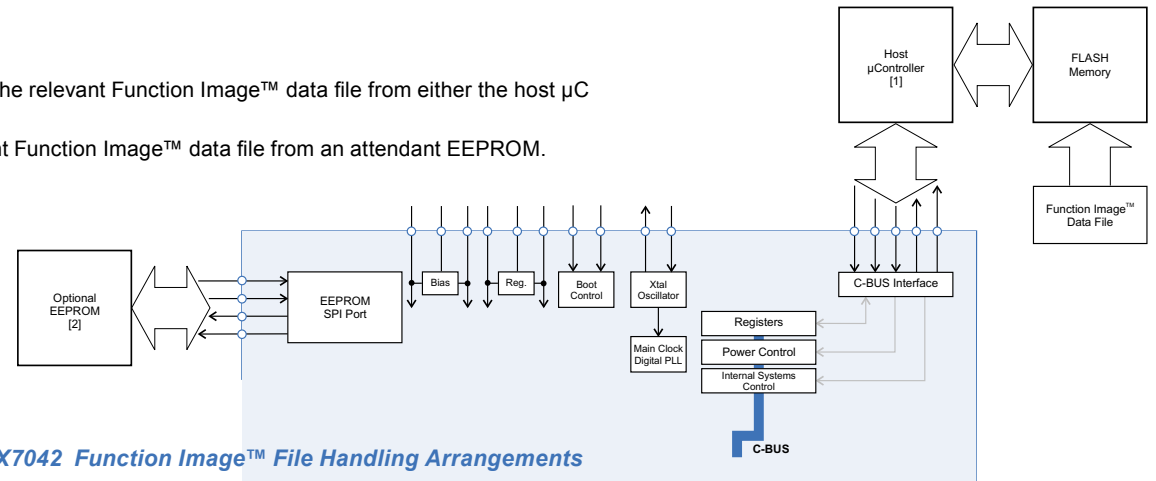
The operational set-up of each product is carried out at the initial power-up of the IC.

- The **CMX910** requires the uploading of a small configuration data file.
- The **CMX7032** and **CMX7042 (FI-1.x)** *FirmASIC*® products require the uploading of the relevant Function Image™ data file from either the host µC or attendant EEPROM.
- The **CMX7032 (FI-2.x)** *FirmASIC*® product only requires the uploading of the relevant Function Image™ data file from an attendant EEPROM. EEPROM contents may be customised prior to loading to the memory.

Full instructions for these processes are given in the IC's datasheet; the required data files are available from the 'MyCML' technical portal on the CML website.

### Function Images (CMX7032 and CMX7042)

- Data Files for IC Configuration
- Downloadable from 'My CML' Technical Portal
- Loaded to IC at Power-Up
- Loaded from µC via C-BUS<sup>[1]</sup> or On-Board EEPROM<sup>[2]</sup>



CMX7032 and CMX7042 Function Image™ File Handling Arrangements

Infinite Capabilities ...

**FirmASIC**®  
... Maximum Flexibility

The **CMX7032** and **CMX7042** products are built on CML's *FirmASIC*® technology.

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a

*FirmASIC*® device are determined by uploading its Function Image™ during device initialisation. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSPs).

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A CML Microsystems Plc Company

## Design Resources

Design and application support is available from: [www.cmlmicro.com/](http://www.cmlmicro.com/)

- Technical Datasheets
- My CML Technical Portal
- Function Image™ File Downloads
- Application Notes
- Evaluation and Development Kits
- AIS Class B Transceiver Reference Design Files
- Frequently Asked Questions
- Application Support via Local Support Desks

## Your Local CML Distributor

[www.cmlmicro.com/company/distribution/](http://www.cmlmicro.com/company/distribution/)